Shoot-Through Control-Based Space Vector Modulation Approach for a Modified Z-Source NPC Power Inverter

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DOI: 10.15598/aeee.v17i4.3514

Abstract. *Z-source Neutral Point Clamped (NPC) inverter is a converter topology that combines the benefits of both the impedance network by storing temporary energy released to the load for voltage boosting and NPC inverter by guaranteeing lower Total Harmonic Distortions (THDs) and reducing voltage stresses of switching devices. In this context, this paper deals with a modified three-level Z-source NPC inverter topology with simplified command to generate shoot-through states and reduce switching losses. For this reason, an extra power switch Insulated Gate Bipolar Transistor (IGBT) is added to insert shoot-through, thus eliminating the need for full-shoot-through on any of the three branches of the inverter. On the other hand, a modified Space Vector Modulation (SVM) strategy is proposed. This gives a number of benefits, both in terms of implementation and harmonic performance. Effectiveness of the proposed topology is verified through simulations using Matlab toolbox Simulation and laboratory experiment.*

Keywords

Shoot through, SVM, Z-source inverter.

1. Introduction

Many manufacturing applications involve higher power inverters, which are usually employed by using multilevel converter technologies. Multilevel converters offer various attractive features including a capacity to produce high voltage waveforms by multilevel step waves, which approximate a sinusoidal wave while the power devices endure only reduced voltages [1].

Several topologies of multilevel inverters have been introduced both in industry and research. In this context, three-level inverters have been receiving more attention from power electronics researchers [2]. Among three-level inverters, the Neutral Point Clamped (NPC) technology can deliver numerous advantages over other topologies such as: lower Total Harmonic Distortions (THDs), reduction of voltage stresses of power devices compared with conventional two-level inverters [3].

However, classical three-level NPC inverter is a step-down converter and it is constrained by its inability of producing an AC output voltage greater than DC-link voltage. Therefore, for renewable energy generation systems where the DC-link voltage is not high enough, a DC-DC boost converter becomes inevitable to boost the DC voltage to produce the required output voltage [4], [5] and [6], but this boost converter increases the cost and complexity of the conversion chain.

Overcoming limitations in three-level NPC inverter, the three-level Z-source NPC inverter with single Z-source network is an emerging topology for power electronics converters with very interesting properties, such as buck–boost characteristics and single-stage conversion with potential for reduced cost, reduced volume, and higher efficiency due to a lower component number [7], [8] and [9].

On the other hand, for emerging power generation technologies, such as fuel cells, photovoltaic arrays, wind turbines, and for new power electronic applications, such as electric and hybrid vehicles, the ZSI is a very promising and competitive topology [10], [11], [12] and [13].

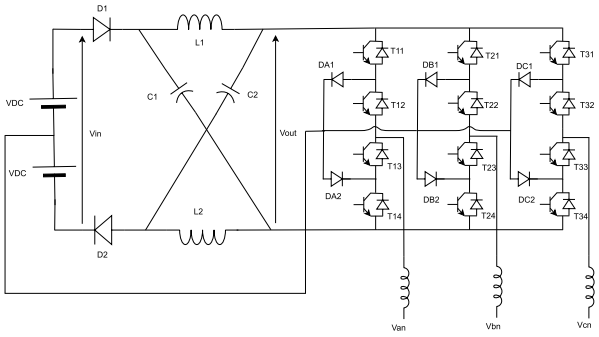


Fig. 1: Scheme of Z-source three-level NPC inverter.

The impedance network mainly consists of two inductors and two capacitors as illustrated in Fig. 1.

The FST for conventional three-level Z-source NPC inverter is done by turning ON all switches in each leg [7], resulting in large pulse of energy loss [14] and [15]; this phenomenon is caused by the intersecting of voltages and currents during each turn-on and turn-off switching moments.

This paper investigates the carrier-based modulation schemes (modified SVPWM) of a modified three-level Z-source NPC inverter topology to reduce switching losses. In this objective, a bidirectional power switch (IGBT) is added as illustrated in Fig. 2, to insert shoot through without need for FST either of three power legs. The theoretical development is discussed in detail, and simulations, as well as experimental results, are used to verify the operation of the circuit and proposed SVM-based modulation.

2. Modified Z-Source NPC Inverter Topology

The configuration of the proposed three-level modified Z-source NPC inverter is illustrated in Fig. 2, where an extra leg consisting of the IGBT is added to the front-end of the three-level NPC inverter bridge.

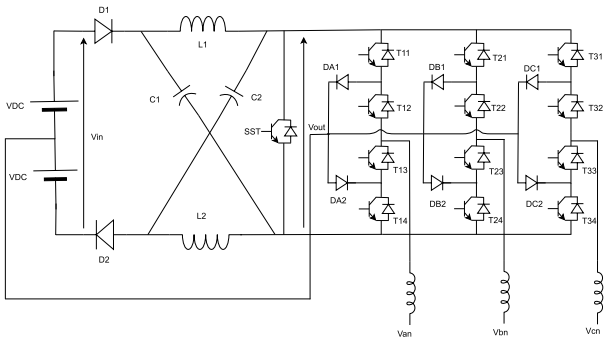


Fig. 2: A modified Z-source three-level NPC inverter.

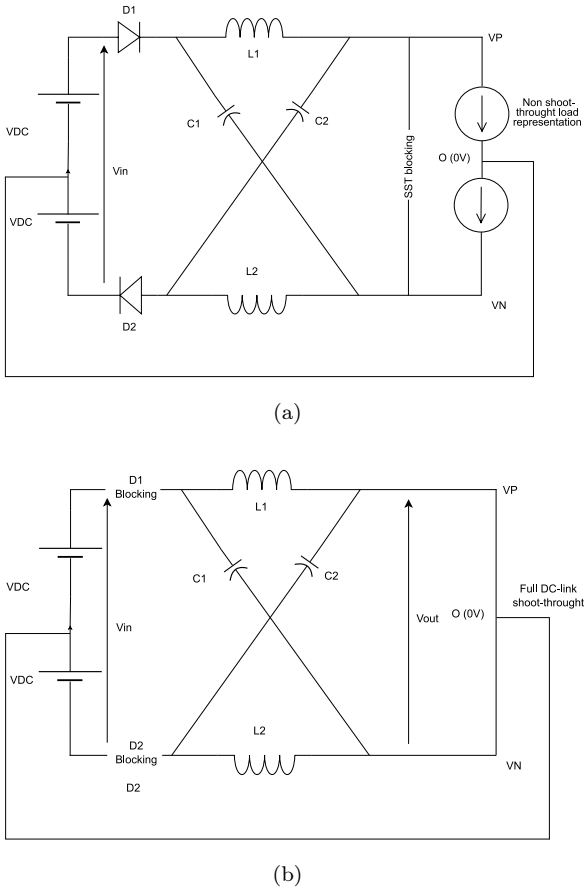


Fig. 3: The modified Z-source three-level NPC inverter in (a) NST and (b) FST.

Tab. 1: Relationship between output line to DC-link midpoint voltage, states of switches and output DC-link voltage.

State type	ON Switches	ON Diode	V_{xy}
NST	SA1, SA'1	D1, D2	$V_{out}/2$
NST	SA'1, SA2	D1, D2, {DA1 or DA2}	0
NST	SA2, SA'2	D1, D2	$-V_{out}/2$
FST	SST	-	0

Figure 3(a) illustrates the NST and Fig. 3(b) illustrates the FST.

Table 1 denotes the relationship between each output line to DC-link midpoint voltage V_{xo} ($x = \{a, b, c\}$), states of switches and output DC-link voltage.

In the following description of the circuit operation, we consider that the Z-source network is symmetrical ($L_1 = L_2 = L$), ($C_1 = C_2 = C$) and the diodes D1 and D2 are identical, capacitor voltages and inductor voltages are typically observed to be the same ($V_{C1} = V_{C2} = V_C$), ($V_{L1} = V_{L2} = V_L$). In NST, the basic circuits shown in Fig. 3(a) with input diodes D1 and D2 are forward biased [8] and [16]. The voltage expressions are as follows:

$$V_L = 2 \cdot V_{dc} - V_C, \tag{1}$$

$$V_{out} = 2 \cdot (V_C - V_{dc}). \tag{2}$$

Otherwise, during the FST by turning ON of SST switch, the basic circuits shown in Fig. 3(b) with input diodes D1 and D2 are reversely biased. The relevant mathematical expressions can be rewritten as:

$$V_L = V_C. \tag{3}$$

Since the average of inductor voltage over a switching cycle T is zero under steady state, from Eq. (1) and Eq. (3) we obtain:

$$(2 \cdot V_{dc} - V_C) \cdot (T - T_{sh}) + V_C \cdot T_{sh} = 0. \tag{4}$$

From Eq. (4), the capacitor voltage is then derived as:

$$V_C = \frac{2V_{dc} \cdot \left(1 - \frac{T_{sh}}{T}\right)}{\left(1 - \frac{2T_{sh}}{T}\right)}. \tag{5}$$

Substituting Eq. (5) into Eq. (2), The peak inverter DC-link voltage $\hat{V}_{out}$ is then derived as:

$$V_{out} = (V_C - V_L) = 2V_C - 2V_{dc} = \frac{2V_{dc}}{\left(1 - \frac{2T_{sh}}{T}\right)}. \tag{6}$$

From Eq. (6), the peak AC output line voltage $\hat{V}_{xo}$ with ($x \in \{a, b, c\}$) for the modified Z-source NPC inverter is derived as follows:

$$\hat{V}_{xo} = M \cdot \frac{\hat{V}_{out}}{2} = M \cdot B \cdot V_{dc}. \tag{7}$$

From Eq. (6) and Eq. (7), it can be found that:

$$G = M \cdot B, \tag{8}$$

where is the voltage gain of the three-level Z-source NPC inverter.

$$B = \frac{1}{1 - 2D}. \tag{9}$$

By setting the denominator of Eq. (9) to zero, the duty ratio can be written as $0 \leq D \leq 0.5$.

The boost factor B is set to unity ($D = 0$) for voltage-buck operation and goes to infinity ($D = 0.5$) for voltage-boost operation.

The duty cycle shoot through is equal to:

$$D = \frac{T_{sh}}{T}. \tag{10}$$

3. Space Vector Pulse Width Modulation of the Modified Z-Source NPC Inverter

Pulse-Width Modulation (PWM) control methods for Z-source three-level NPC inverter have been proposed to reach the maximum voltage with the lowest THD in the output voltages. Two widely used PWM methods are the carrier-based Sine wave Pulse Width Modulation (SPWM) and the Space Vector Modulation (SVM). This study focuses on SVM as the modulation method for the modified Z-source NPC inverter in hope that it offers the same advantages when applied to conventional NPC inverter (SVM has 15 % higher utilization ratio of the V_{dc} voltage, low current ripple and relatively easy hardware implementation) [17].

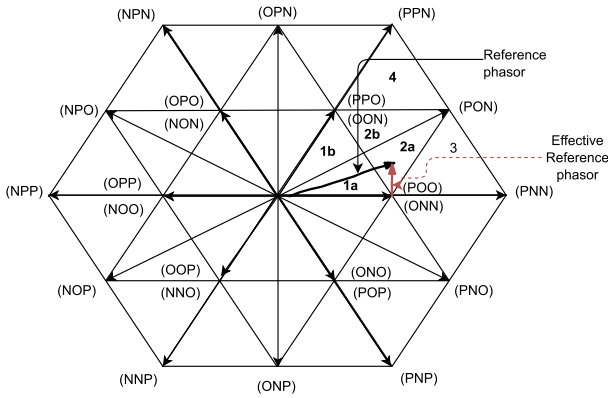


Fig. 4: Space vector representation of a three-level inverter.

The SVM is a PWM strategy that uses the concept of space vectors to calculate the triggering time of each power switch. The operation of each inverter phase leg of a traditional three-level NPC inverter can be denoted by three switching states P, O, and N. Taking all three phases into account, the inverter has a total of twenty-seven switching states. Figure 4 illustrates the hexagon related to the three-level NPC inverter and denotes all the possible 27 switching states; the rotating reference vector $\vec{V}_{ref}$ represents the desired three-phase output voltage [17].

The SVM for the NPC inverter is based on the "volt-second balancing" principle; that is, the product of the reference voltage and the sampling period equals the sum of the voltage multiplied by the time interval of chosen space vectors. The "volt-second balancing" principle enables us to calculate the duty cycle of the various space vectors over a switching period. Applying the selected voltage vectors to the output according to a switching sequence completes the modulation process. A switching sequence that gives minimum number of switching transitions and high-quality output waveform is the preferred choice [18].

The reference vector $\vec{V}_{ref}$ can be expressed as:

$$V_{ref} = \frac{2}{3} \cdot \left(V_{ao}(t)e^{j0} + V_{bo}(t)e^{j\frac{2\pi}{3}} + V_{co}(t)e^{j\frac{4\pi}{3}} \right). \tag{11}$$

Generally, in SVM, the reference vector $\vec{V}_{ref}$ is synthesized with Nearest Three Vectors Space Modulation Strategies (NTV SVM), which are selected based on the triangle, in which the reference vector is located at the sampling instant [19]. If the reference vector is located in triangle 2, the nearest three vectors are: $\vec{V}_1, \vec{V}_2$ and $\vec{V}_7$, respectively.

Let the duty ratios of these vectors be denoted by d_0, d_1 and d_2, respectively. The modulation law with a sequence of the nearest three vectors based on the volt-second product is then as follows:

$$d_0 \cdot \vec{V}_1 + d_1 \cdot \vec{V}_2 + d_2 \cdot \vec{V}_7 = \vec{V}_{ref}, \tag{12}$$

$$d_0 + d_1 + d_2 = 1. \tag{13}$$

The voltage vectors $\vec{V}_1, \vec{V}_2, \vec{V}_7$ and $\vec{V}_{ref}$ appeared in Fig. 4 can be expressed as:

$$\vec{V}_1 = \frac{2}{3} V_{dc} e^{j0}, \tag{14}$$

$$\vec{V}_2 = \frac{2}{3} V_{dc} e^{j\frac{\pi}{3}}, \tag{15}$$

$$\vec{V}_7 = \frac{2}{\sqrt{3}} V_{dc} e^{j\frac{\pi}{6}}, \tag{16}$$

$$\vec{V}_{ref} = V_{ref} e^{j\theta}. \tag{17}$$

By substituting Eq. (14), Eq. (15), Eq. (16) and Eq. (17) into Eq. (12), the duty ratios of the nearest three voltage vectors are given by:

$$\begin{cases} t_0 = T_s \cdot \left[2 - 2 \cdot M \sin\left(\frac{\pi}{3} + \theta_{ref}\right) \right] \\ t_1 = T_s \cdot \left[2 \cdot M \sin\left(\frac{\pi}{3} + \theta_{ref}\right) \right] \\ t_2 = T_s \cdot \left[2 \cdot M \sin\left(\frac{\pi}{3} - \theta_{ref}\right) - 1 \right] \end{cases}, \tag{18}$$

where $\left(M = \frac{\sqrt{3} \cdot V_{ref}}{V_{dc}} \right)$ is the modulation index and $0 \leq \theta_{ref} \leq \frac{\pi}{3}$ is the angle of the reference vector within the sector.

A similar procedure is used to derive the duty ratios of the selected voltage vectors for the other triangles.

To complete the modulation process, the selected voltage vectors are applied to the output according to a switching sequence.

To attain the least number of switches changing between two nearby states, a seven-segment switching sequence is implemented in SVM. If the reference vector stays in triangle 2 as is shown in Fig. 4, by using the decomposition method, where the center of hexagon is moved from {PPP/OOO/NNN} to {POO/ONN}, the null vector (E-null) is transferred to {POO/ONN} while the active vectors are transferred to {PPO/OON} and PON, respectively [8].

The seven-segment switching sequence in triangle 2 can then be illustrated as shown in Tab. 2.

In order to achieve boost functionality for three-level Z-source NPC inverter, shoot-through states are inserted into the appropriate phase legs. However, in the modified Z-source NPC inverter proposed in this study, only one leg consisting of one switch IGBT (SST) is Solicited to insert Shoot-Through.

Tab. 2: Seven-segment switching sequence in triangle 2.

	Segment	Vector	State
E-null	1st	$\vec{V}_1$	ONN
E-active1	2nd	$\vec{V}_2$	OON
E-active2	3rd	$\vec{V}_7$	PON
E-null	4th	$\vec{V}_1$	POO
E-active2	5th	$\vec{V}_7$	PON
E-active1	6td	$\vec{V}_2$	OON
E-null	7th	$\vec{V}_1$	ONN

A seven-segment switching sequence after insertion of shoot-through is shown in Tab. 3.

Tab. 3: Seven-segment switching sequence for three-level Z-source NPC inverter when $\vec{V}_{ref}$ is located in triangle 2 of sector 1.

	Segment	Vector	State
E-null	1st	$\vec{V}_1$	ONN
FST			FST
E-active1	2nd	$\vec{V}_2$	OON
E-active2	3rd	$\vec{V}_7$	PON
FST			FST
E-null	4th	$\vec{V}_1$	POO
FST			FST
E-active2	5th	$\vec{V}_7$	PON
E-active1	6td	$\vec{V}_2$	OON
FST			FST
E-null	7th	$\vec{V}_1$	ONN

The conventional FST operation mode requires all four switches in phase to be turned ON. This is not a minimal loss approach since, for example, switching phase A from U_c to 0 V would require switches {SA1, SA'1, SA2, SA'2} changing from {ON, ON,

OFF, OFF} through {ON, ON, ON, ON} to {OFF, ON, ON, OFF}.

In the modified three-level Z-source NPC inverter, FST operation mode requires only the added leg to be turned ON. Then, switching phase A from U_c to 0 V requires switches {SA1, SA'1, SA2, SA'2} changing from {ON, ON, OFF, OFF} to {OFF, ON, ON, OFF} directly, which is a minimal loss approach.

The zero state repeats periodically every $\frac{\pi}{3}$, so the average zero state duty ratio over one cycle can be expressed by:

$$\frac{T_0}{T} = \frac{1}{\pi/3}\int_0^{\frac{\pi}{3}} \left[2 - 2\cdot M \sin\left(\frac{\pi}{3} + \theta_{ref}\right)\right] = \\ = 2 - \frac{6\cdot M}{\pi}. \tag{19}$$

From Tab. 3, the shoot-through state is equally divided into four parts produced during the time intervals of zero vectors, from Eq. (19) the maximum of shoot-through duty ratio is:

$$D_{\max} = \frac{\left(2 - \frac{6\cdot M}{\pi}\right)}{2}. \tag{20}$$

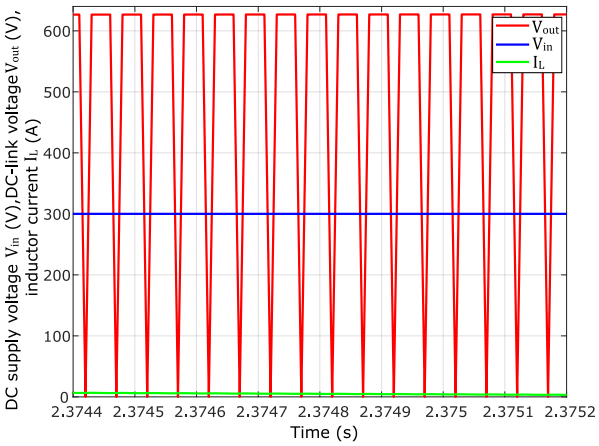
4. Simulation Results

Extensive simulations were carried out on Matlab/Simulink in order to verify the robustness of the modified SVM strategy applied on the modified topology of Z-source NPC inverter. The parameters of the simulated circuit are: DC-link voltage V_{in} = 300 V, Z-source network inductor and capacitor 9.6 mH and 4700 μF, respectively. The switching frequency is 2 kHz, modulation index M = 0.8. The parameters of the induction motor (as a load for the studied inverter) are given in appendix.

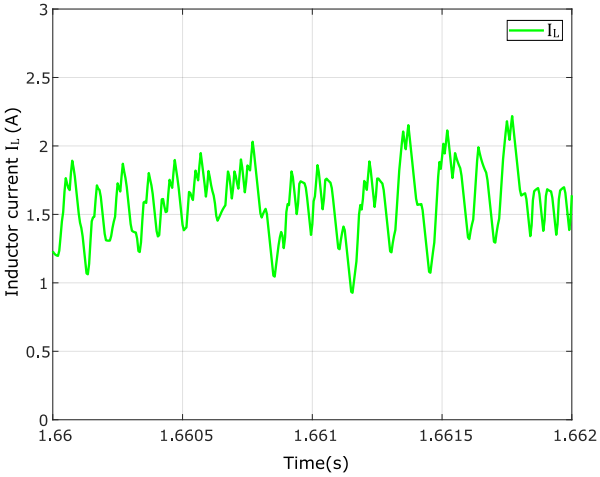
The waveform of DC-link voltage V_{in} and DC-link voltage V_{out} of the Z-source inverter are shown in Fig. 5(a). It can be seen that the amplitude of DC-link voltage V_{out} is 628 V, in accordance with the theoretical analysis ($\hat{V}_{out} = V_{in} \cdot B = 621$ V).

The waveform of the inductor current I_L using the SVM control method is shown in Fig. 5(b). It presents ripple due to the inductance of the Z-source structure. It can be seen that the inductor current is increased during the shoot-through state, which proves that the two inductors have been charged in moment of shoot-through. However, during active states, this current is decreased because the two inductors have been discharged. The energy stored in the inductors is released to the external AC load.

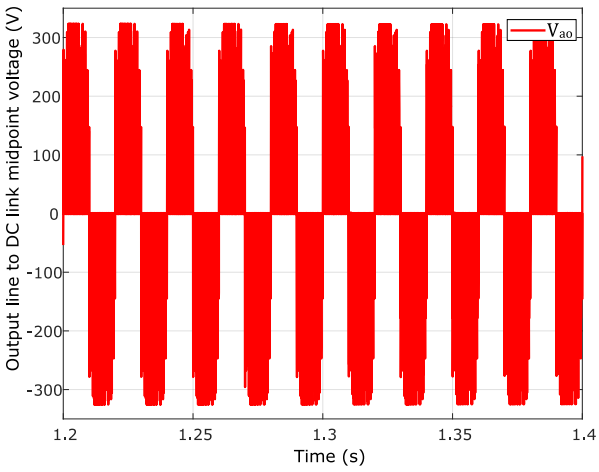
The line-to-line voltage waveforms with five levels and line-to-neutral waveforms with three voltage levels are shown in Fig. 5(c) and Fig. 5(d) respectively. It can be seen that the amplitudes of both voltages have been boosted up to about 628 V and 315 V respectively, which is in accordance with the theoretical analysis.



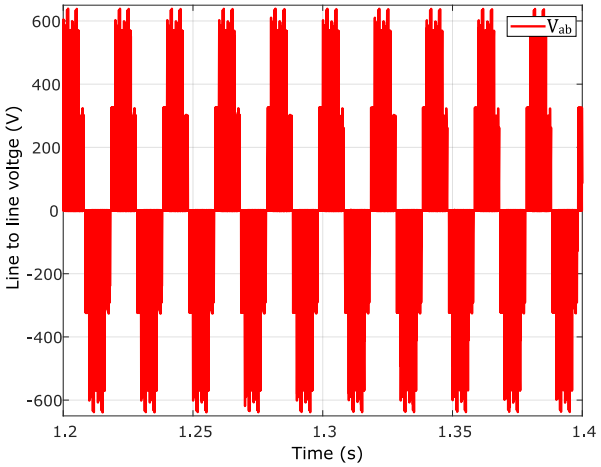
(a) DC supply voltage V_{in}, DC-link voltage V_{out} and inductor L current I_L.



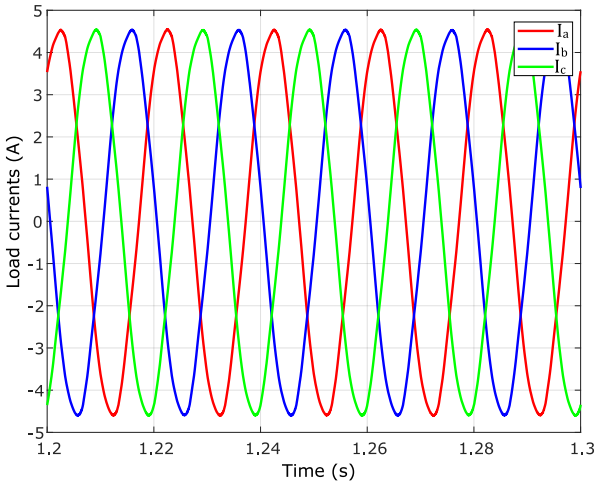
(b) Inductor L current I_L.



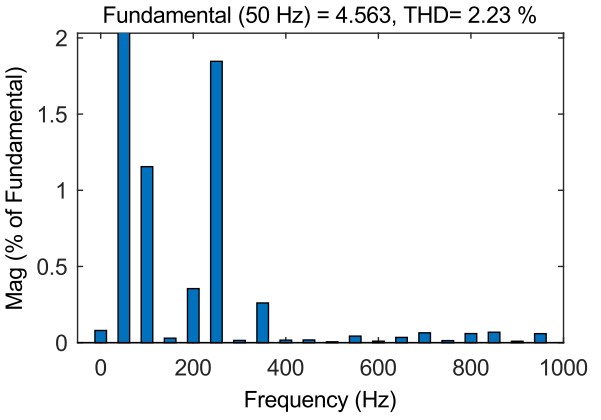
(c) Output line to DC link midpoint voltage V_{ao}.



(d) Line to line voltage V_{ab}.



(e) Load currents I_a, I_b, and I_c.



(f) Harmonic spectrum of load current.

Fig. 5: Simulation results of the three-level Z-source NPC SVM control (with $M = 0.8, B = 2.07,$ THD $= 52.53$ %).

The load currents waveforms and spectrum of the load current I_a are shown in Fig. 5(e) and Fig. 5(f) respectively. It can be seen that the modified Z-source NPC inverter is able to produce sinusoidal, balanced currents with lower THD of 2.83 %.

Finally, these simulation results confirm and verify the benefits of the proposed modulation strategy.

5. Experimental Results

The experimental test bench, illustrated by Fig. 6, consists of a three-level NPC inverter and the impedance source network, whose parameters are given in the Appendix. The experimental prototype gating signals were generated by PCE card.

Waveforms of the Z-source capacitor voltages are shown in Fig. 7(a). It can be seen that these voltages have been boosted to the required value ($\hat{V}_{out} = V_{in} \cdot B = 2.1 \cdot V_{in}$ Volts). The corresponding experimental result, shown in Fig. 7(a), is very close to the simulated waveform (see Fig. 5(a)).

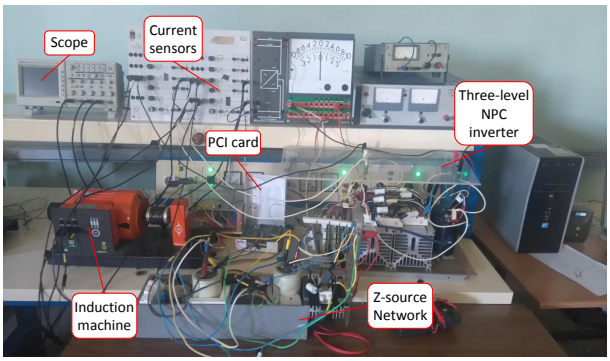
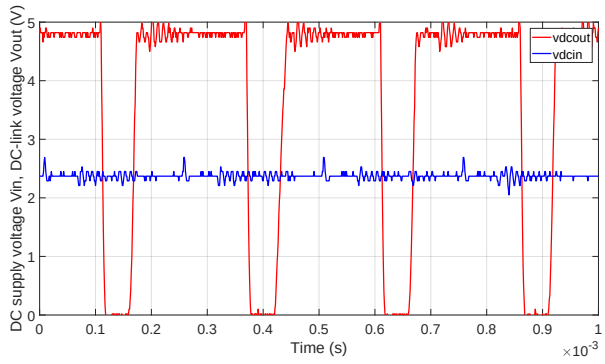


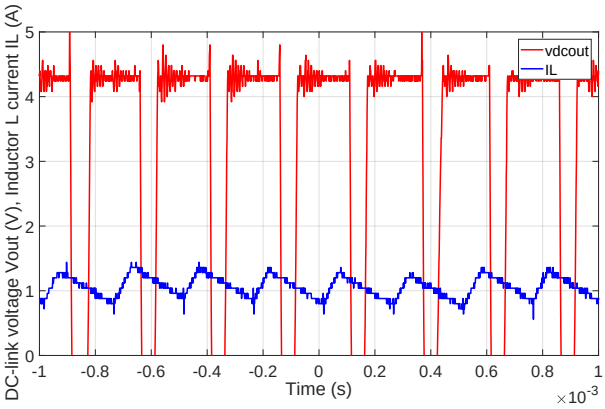
Fig. 6: The experimental setup.

The waveform of the inductor current I_L using the SVM control method is shown in Fig. 7(b). It can be seen that the inductor current is increased during the shoot-through state. However, during active states, this current is decreased because the two inductors has been discharged. The corresponding experimental result, shown in Fig. 7(b), is very close to the simulated waveform (see Fig. 5(b)).

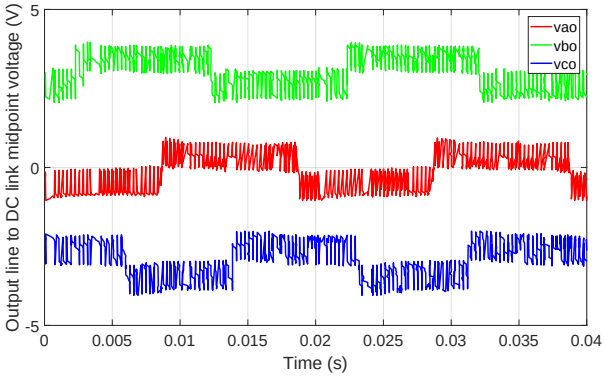
The achieved results shown in Fig. 7(c) and Fig. 7(d) have demonstrated the ability of the modified Z-source NPC inverter to generate multilevel output voltages and perform voltage buck-boost operation with the modified SVM technique. The presented results match well the theoretical analysis.



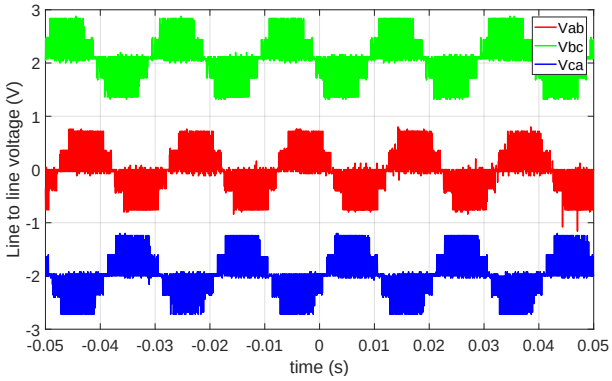
(a) DC supply voltage V_{in}, DC-link voltage V_{out}.



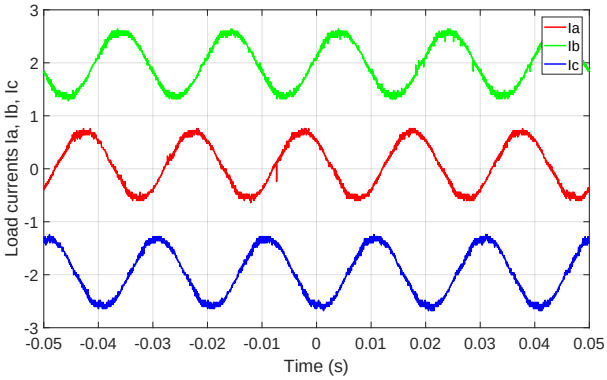
(b) DC-link voltage V_{out} and Inductor L current I_L.



(c) Output line to DC link midpoint voltage V_{ao}.



(d) Line to line voltage V_{ab}.



(e) Load currents I_a, I_b, and I_c.

Fig. 7: Experimental results of the three-level Z-source NPC using SVM control (with $M = 0.8, B = 2.07$).

The load currents are also shown in Fig. 7(e). It is noted that the load currents remain sinusoidal and balanced in the boost mode with the experimental waveforms matching the simulation waveforms closely.

6. Discussion and Conclusion

This paper has proposed a modified Z-source inverter. This converter is able to perform voltage buck-boost function by introducing only one shoot-through state in each null state via acting on the extra fourth leg, which means reduction in time calculation and minimization of the stress on the switches of the inverter leg.

The ability of the modified Z-source NPC inverter to generate multilevel output voltages and perform voltage buck-boost operation with SVM strategy have been demonstrated with the results both in simulation and experiment. The ability of the modified Z-source NPC inverter to produce sinusoidal, balanced currents with lower THD is also verified.

Similarly, the split DC-link voltages applied to the back-end of the modified Z-source NPC inverter are shown in the simulated and experimental conditions. By comparing the simulation and experimental results, one finds a close matching between the simulation and experimental results.

The number of commutations in order to create shoot-through-state in the modified Z-source NPC inverter is still lower compared with shoot-through-states in conventional Z-source NPC inverter.

Table 4 summarizes the maximum shoot-through duty ratio $D_{\max}$, boost factor, voltage gain, inductor current ripples and the THD of line current when using SVM strategy to insert shoot-through-states in the modified Z-source NPC inverter.

Tab. 4: Shoot-through duty ratio D, boost factor (B), voltage gain (G), and inductor current ripples (ΔI_L).

Control strategies	MSVM	
	Theoretical	Practical
D_{sh}	0.23	0.2
B	2.07	2
G	1.656	1.6
ΔI_L (A)	$1-3$	1.5
Current THD	2.83 %	-

Voltage drop on the passive components and power semiconductor devices mainly causes the differences between the experimental results and expected values.

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Appendix

Nomenclature

IGBT	=	Isolated Gate Bipolar Transistors,
DC	=	Direct Current,
SST	=	Switch for Shoot-Through,
NST	=	Non Shoot-Through,
ZSI	=	Z-source Inverter,
FST	=	Full-Shoot-Through,
SVPWM	=	Space Vector Pulse Width Modulation,
NTV	=	Nearest Three Vectors,
THD	=	Total Harmonic Distortion,
NPC	=	Neutral Point Clamped,
V_{dc}	=	DC-link voltage,
VSIs	=	Voltage Source Inverters,
V_{C1}, V_{C2}, V_C	=	Average Z-source capacitor voltage,
V_{xy}	=	Peak fundamental AC line-to-line voltage,
ΔIL	=	Current ripple in inductor,
D	=	Duty cycle Shoot-Through,
B	=	Boost Factor,
G	=	Voltage Gain,
T	=	Switching Period,
T_{sh}	=	Shoot-through duration,
L_1, L_2	=	Z-source inductors,
C_1, C_2	=	Z-source capacitors,
V_p	=	Upper shoot-through envelope,
V_n	=	Lower shoot-through envelope,
i_{DC}	=	DC current,
V_{AO}, V_{BO}, V_{CO}	=	Output line to DC-link midpoint voltage,
I_A, I_B, I_C	=	load currents,
V_{AB}, V_{BC}, V_{CA}	=	Output Line to line input voltage,
V_{ref}	=	Reference output voltage vector.

Inductance and Capacitor Network

- L = 9.6 mH,
- C = 5500 μF.

Rated Data of the Tested Induction Motor

- $P = 1$ kW, 2.5 Nm,
- $\Omega = 2830$ rpm,
- $p = 1$,
- $R_s = 4.750\ \Omega$,
- $R_r = 8.000\ \Omega$,
- $L_s = 0.375$ H,
- $L_r = 0.375$ H,
- $M = 0.364$ H,
- $J = 0.003$ kg·m^2,
- $k_f = 0.0024$ Nm.